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Description

MODIFICATION OF ELECTRICAL PROPERTIES FOR SEMICONDUCTOR WAFERS

BACKGROUND ART

[0001] 1. Technical Field

[0002] The present invention relates to a structure and associated method for manufacturing a plurality of semiconductor wafers.

[0003] 2. Related Art

[0004] The fabrication of microelectronic devices requires multiple processing steps. Some of these steps influence electrical characteristics of these devices. Variability in a process often results in unacceptable variability in the devices. Thus, there exists a need to control or eliminate variability of certain critical processing steps.

[0005] Summary of the Invention

[0006] The present invention provides a method of fabricating semiconductor wafers, comprising:

providing a plurality of semiconductor wafers, wherein the plurality of semiconductor wafers comprises a first semiconductor wafer and a second semiconductor wafer, and wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer;

providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials;

choosing a material from the plurality of materials existing in said relationship;

forming a substructure comprising the material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the of the second semiconductor wafer; and

placing the plurality of semiconductor wafers into a furnace for processing, wherein the furnace comprises an elevated temperature resulting in a value for the first semiconductor wafer of the electrical characteristic that corresponds to said material in said relationship.

[0007]

The present invention provides a method of fabricating semiconductor wafers, comprising:

providing a plurality of semiconductor wafers, wherein the plurality of semiconductor wafers comprises a first semiconductor wafer, a second semiconductor wafer, a third semiconductor wafer, and a forth semiconductor wafer, wherein the first semiconductor wafer is located adjacent to the second semiconductor wafer, and wherein the third semiconductor wafer is located adjacent to the forth semiconductor wafer;

providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials;

choosing a first material from the plurality of materials existing in said relationship;

choosing a second material from the plurality of materials existing in said relationship;

forming a first substructure comprising the first material sandwiched between a topside of the first semiconductor wafer and a backside of a portion of the of the second semiconductor wafer;

forming a second substructure comprising the second material sandwiched between a topside of the third semiconductor wafer and a backside of a portion of the of the forth semiconductor wafer;

placing the plurality of semiconductor wafers into a furnace for processing, wherein

the furnace comprises an elevated temperature resulting in a first value for the first semiconductor wafer of the electrical characteristic that corresponds to said first material in said relationship and a second value for the third semiconductor wafer of the electrical characteristic that corresponds to said second material in said relationship, and wherein the first value is not a same value as the second value.

[0008] The present invention provides an electrical structure, comprising:
a first semiconductor wafer;
a second semiconductor wafer; and
a first material, wherein the first material is sandwiched between a topside of the first semiconductor wafer and a backside of the of the second semiconductor wafer, wherein a relationship exists between a plurality of values for an electrical characteristic and a plurality of materials comprising the first material, and wherein the first semiconductor wafer comprises a discrete value from the plurality of values for the electrical characteristic that correlates with the first material in said relationship.

[0009] The present invention advantageously provides a method and associated structure to control or eliminate variability of certain critical processing steps during a fabrication of microelectronic devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 illustrates a front cross-sectional view of a first semiconductor wafer and a second semiconductor wafer, in accordance with embodiments of the present invention.

[0011] FIGS. 2A and 2B illustrate an alternative to FIG. 1, in accordance with embodiments of the present invention.

[0012]
FIG. 3 illustrates an alternative to FIGS. 1, 2A, and 2B, in accordance with

embodiments of the present invention.

[0013] FIG. 4 is a flowchart depicting an algorithm for the wafer/semiconductor device manufacturing process of FIGS. 1-3, in accordance with embodiments of the present invention.

[0014] FIG. 5 illustrates a perspective view of a plurality of wafers in a wafer holder for placement in a furnace for a wafer/semiconductor device manufacturing process, in accordance with embodiments of the present invention.

[0015] Fig. 6 illustrates a graph for providing a first relationship between a plurality of values for an electrical characteristic, in accordance with embodiments of the present invention.

[0016] Fig. 7 illustrates a graph for providing a second relationship between a plurality of values for an electrical characteristic, in accordance with embodiments of the present invention.

[0017] Fig. 8 illustrates a graph of laboratory test data showing polysilicon sheet resistance verses various semiconductor wafers, in accordance with embodiments of the present invention.

[0018] Fig. 9 illustrates a graph of laboratory test data showing Gate oxide thickness verses various semiconductor wafers, in accordance with embodiments of the present invention.

DISCLOSURE OF INVENTION

[0019]

FIG. 1 illustrates a front cross-sectional view of a first semiconductor wafer 4 and a second semiconductor wafer 7, in accordance with embodiments of the present invention. The first semiconductor wafer 4 comprises a topside 8 and a backside 10. The second semiconductor wafer 7 comprises a topside 12 and a backside 15. The

term TOPSIDE of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that comprises or will comprise (i.e., through a wafer/semiconductor device manufacturing process) active electrical components (e.g., transistors, resistors, capacitors, etc.) and/or conductive wiring between active electrical components. The term BACKSIDE of a semiconductor wafer (e.g., backside 10 of the semiconductor wafer 4 and backside 15 of the semiconductor wafer 7) is defined herein including in the claims as a surface of a semiconductor wafer that does not comprise active electrical components (e.g., transistors, resistors, capacitors, etc.). The term WAFER/SEMICONDUCTOR DEVICE MANUFACTURING PROCESS is defined herein as a process to form a layer(s) of a material (i.e., for producing active electrical components, a mask, a junction (for transistors), an insulating layer, etc.) on a top side of a semiconductor wafer (e.g., topside 8 of the semiconductor wafer 4 and topside 12 of the semiconductor wafer 7). Any wafer/semiconductor device manufacturing process known to a person of ordinary skill in the art may be used for the present invention including, inter alia, diffusion, chemical vapor deposition (CVD) processing, etc. During a CVD process a furnace provides an environment comprising a high temperature (e.g., about 500°C to about 650°C) and a controlled gas flow to form the layer(s) of a material. Gases used during a CVD process may include, inter alia, SiH4, nitrogen, etc. During diffusion process a furnace is used to expose the semiconductor wafer to an oxidizing environment at an elevated temperature (e.g., about 600°C to about 1300°C) to form the layer(s) of a material. Gases used during a diffusion process may include, inter alia, oxygen, nitrogen, nitrous oxide, hydrogen, etc. During a wafer/semiconductor device manufacturing process, a layer formation (i.e., for producing active electrical components, a mask, a junction (for transistors), an insulating layer, etc.) on a first wafer (e.g., wafer 7) is modulated by a material (e.g., layer 21) that is adjacent to a topside (e.g., topside 12) of the first

wafer (e.g., wafer 7) thereby producing values of an electrical characteristic(s) (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) that are dependent upon the material (e.g., layer 21). For example, the semiconductor wafer 4 comprises a film layer 21 of a specified material attached to the backside 10. The film layer 21 comprising the specified material may be selected by providing a relationship between a plurality of values for an electrical characteristic and a plurality of materials (see FIGS. 6-9). The relationship may be, inter alia, graphical (as shown in FIGS. 6 and 7), tabular, etc. The specified material comprised by the film layer 21 may be any material including, inter alia, Si, Si3N4, SiO2, etc. The film layer 21 comprising the specified material is applied to the backside 10 of the semiconductor wafer 4 so that during the wafer/semiconductor device manufacturing process a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7 may be obtained. Therefore specific discrete values for electrical characteristics of active electrical components (e.g., resistance (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) may be selected based upon specific materials selected (i.e., using the a relationship between a plurality of values for an electrical characteristic and a plurality of materials as shown in FIGS. 6 and 7). Based on a desired value for electrical characteristics of active electrical components, the film layer 21 (comprising a specific material) may be applied (i.e., coupled) to the backside 10 of the semiconductor wafer 4 prior to the wafer/semiconductor device manufacturing process as shown in FIG. 1. Alternatively a film layer may be removed (in a case where a semiconductor wafer comprises a plurality of film layers) to expose a film layer comprising a specific material as shown in FIGS. 2A and 2B.

[0020] FIGS. 2A and 2B illustrate an alternative to FIG. 1 showing the front cross-sectional view of a first semiconductor wafer 4 and a second semiconductor wafer 7, in accordance with embodiments of the present invention. In contrast to FIG. 1, FIG. 2A comprises a first film layer 24 and a second film layer 21. The first film layer 24 and the second film layer 21 each comprise a different material. The first film layer 24 may comprise any material including, inter alia, Si, Si3N4, SiO2, etc. The second film layer 21 may comprise any material including, inter alia, Si, Si3N4, SiO2, etc. In FIG. 2B the second film layer 21 has been removed so that the first film layer 24 is exposed and adjacent to the topside 12 of the semiconductor wafer 7. A material comprised by the first film layer 24 will produce a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7 during the wafer/semiconductor device manufacturing process. The material used to produce the desired value is selected using the a relationship between a plurality of values for an electrical characteristic and a plurality of materials as shown in FIGS. 6 and 7.

[0021]

FIG. 3 illustrates an alternative to FIGS. 1, 2A, and 2B showing a front cross-sectional view of a first semiconductor wafer 4, a second semiconductor wafer 7, and a filler wafer 28, in accordance with embodiments of the present invention. In contrast to FIGS. 1, 2A, and 2B, FIG. 3 comprises a filler wafer 28 (instead of a film layer (e.g., film layer 21 in FIG. 1 or film layer 24 in FIG. 2B) for producing the desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7 during the wafer/semiconductor device manufacturing process. The filler wafer is placed

between a backside 10 of the semiconductor wafer 4 and a topside 12 of the semiconductor wafer 7. The filler wafer 28 any material including, inter alia, Si, Si3N4, SiO2, etc. The material used to produce the desired value is selected using the a relationship between a plurality of values for an electrical characteristic and a plurality of materials as shown in FIGS. 6 and 7.

[0022] FIG. 4 is a flowchart depicting an algorithm 37 for the wafer/semiconductor device manufacturing process of FIGS. 1-3, in accordance with embodiments of the present invention. In step 39 a plurality of wafers are provided. In step 40 a decision is made as to whether or not a desired (specific) value for an electrical characteristic (s) (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) is required. If a desired value is not required in step 40 then the wafers are subjected to a wafer/semiconductor device manufacturing process. If a desired value is required in step 40 then a relationship between a plurality of values for an electrical characteristic and a plurality of materials must be developed (as shown in FIGS. 6 and 7) in step 42. The relationship may be, inter alia, graphical (as shown in FIGS. 6 and 7), tabular, etc. In step 43 the desired value and associated material to produce the desired value during a wafer/semiconductor device manufacturing process is selected using the relationship developed in step 42. In step 44 a method of adding the associated material to produce the desired value of an electrical characteristic(s) (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) will be determined.

[0023] If the method of FIG. 1 is selected in step 44 then step 50 is executed such that the film layer 21 (see FIG. 1) is applied (i.e., coupled) to the wafer 4 (such that the film layer 21 is sandwiched between the topside 12 of the semiconductor wafer 7 and a backside 10 the semiconductor wafer 4). In step 52, the wafers 4 and 7 are placed in a furnace for a wafer/semiconductor device manufacturing process thereby

producing a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component (s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7.

[0024] If the method of FIG. 2 is selected in step 44 then step 46 is executed such that the film layer 21 (see FIG. 2) is removed from the wafer 4 thereby exposing the film layer 21 (coupled to the semiconductor wafer 4) to the topside 12 of the semiconductor wafer 7. In step 56 the wafers 4 and 7 are placed in a furnace for wafer/semiconductor device manufacturing process thereby producing a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7.

[0025] If the method of FIG. 3 is selected in step 44 then step 48 is executed such that the filler wafer 28 (see FIG. 3) is placed (i.e., without attaching to wafer 4 or 7) between the backside 10 of the wafer 4 and the topside 12 of the wafer 7. In step 54, the wafers 4 and 7 and the filler wafer 28 are placed in a furnace for wafer/semiconductor device manufacturing process in step 54 thereby producing a desired value (i.e., a controlled value) of an electrical characteristic (e.g., resistance such as polysilicon sheet resistance, capacitance, gate oxide thickness, threshhold voltage, standby current, etc) for active electrical component(s) (e.g., transistors, resistors, capacitors, etc.) on the topside 12 of the semiconductor wafer 7.

[0026] FIG. 5 illustrates a perspective view of a plurality of wafers 63 in a wafer holder 64 for placement in a furnace 62 for wafer/semiconductor device manufacturing process, in accordance with embodiments of the present invention. The plurality of wafers 63 may include a film layer 65 similar to the film layer 21 applied to the wafer

4 and the wafer 7 of FIG. 1. Alternatively, the film layer 65 could be replaced by a film layer analogous to the film layer 24 exposed to the wafer 7 of FIG. 2, the filler wafer 28 between the wafer 4 and the wafer 7 of FIG. 3, or any combination thereof. The wafer holder 64 may comprise any wafer holder material known to a person of ordinary skill in the art including, inter alia, quartz, silicon carbide, etc. The furnace 62 may be any wafer processing furnace known to a person of ordinary skill in the art including, inter alia, PolysiliconLPCVD furnace, a gate oxidation furnace, etc.

[0027] Fig. 6 illustrates a graph for providing a first relationship (graphical) between a plurality of values for an electrical characteristic (i.e., polysilicon resistance) and a plurality of materials so that a specific value for an electrical characteristic may selected based on a material selected, in accordance with embodiments of the present invention. The Y-axis represents values for polysilicon resistance in arbitrary units. The X-axis represents the plurality of materials (i.e., Si, Si3N4, and SiO2). The values for polysilicon resistance with respect to a material (i.e., Si, Si3N4, and SiO2) are represented by data points 67, 68, and 69. As illustrated by the data points 67, 68, and 69, it may be determined that the polysilicon resistance values increase as the materials change from Si to Si3N4 to SiO2. Additionally, any combination of materials (i.e., Si, Si3N4, and SiO2) may be used to provide values for polysilicon resistance that fall between the data points 67, 68, and 69.

[0028] Fig. 7 illustrates a graph for providing a second relationship (graphical) between a plurality of values for an electrical characteristic (i.e., gate oxide thickness) and a plurality of materials so that specific value for an electrical characteristic may selected based on a material selected, in accordance with embodiments of the present invention. The Y-axis represents values for gate oxide thickness in arbitrary units. The X-axis represents the plurality of materials (i.e., Si, Si3N4, and SiO2). The values for gate oxide thickness with respect to a material (i.e., Si, Si3N4, and SiO2) are represented by data points 71, 72, and 73. As illustrated by the data

points 71, 72, and 73, it may be determined that the gate oxide thickness increases as the materials change from Si to Si3N4 to SiO2. Additionally, any combination of materials (i.e., Si, Si3N4, and SiO2) may be used to provide values for gate oxide thickness that fall between the data points 71, 72, and 73.

[0029] Fig. 8 illustrates a graph of laboratory test data showing polysilicon sheet resistance verses various semiconductor wafers W1-W23 with various materials placed above the semiconductor wafers W1-W23 during a wafer/semiconductor device manufacturing process, in accordance with embodiments of the present invention. The semiconductor wafers W1-W23 were placed in a polysilicon LPCVD furnace for 20 minutes at a temperature of 620° C and a pressure of 150 milliTorr. The semiconductor wafers W1-W23 each comprise a same material (e.g., polysilicon, etc). The X-axis represents the semiconductor wafers W1-W23. The Y-axis represents resistance in ohms. The values for resistance for semiconductor wafers W1-W23 with various materials placed above the semiconductor wafers W1-W23 are represented by the data points 101, 102,...,115...,123. Data points 102, 103, ...114, 116...123 represent values of resistance (about 1380 ohms + 30) for semiconductor wafers comprising a layer of SiO2 above them. Data point 101 represents a value of resistance (about 1225 ohms/ف) for a semiconductor wafer comprising a layer of Si3N4 above. Data point 115 represents a value of resistance (about 1135 ohms/ف) for a semiconductor wafer comprising a layer of Si above. As illustrated by the data points 101, 102,...,115...,123 it may be determined that the polysilicon sheet resistance values increase as the materials change from Si to Si3N4 to SiO2 and that based on a material placed above a semiconductor wafer during a wafer/semiconductor device manufacturing process a value of an electrical characteristic (e.g., polysilicon sheet resistance) may be changed.

[0030] Fig. 9 illustrates a graph of laboratory test data showing Gate oxide thickness verses various semiconductor wafers V1-V15 with various materials placed above

the semiconductor wafers V1-V15 during a wafer/semiconductor device manufacturing process, in accordance with embodiments of the present invention. The semiconductor wafers V1-V15 were placed in a gate oxidation furnace for 60 minutes at a temperature of 800° C degrees and a pressure of 760 Torr. The semiconductor wafers V1-V15 each comprise a same material (e.g., silicon oxynitride). The X-axis represents the semiconductor wafers V1-V15. The Y-axis represents gate oxide thickness in angstroms. The values for gate oxide thickness for semiconductor wafers V1-V15 with various materials placed above the semiconductor wafers V1-V15 are represented by the data points 201, 202,...215. Data points 202...215 represent values of gate oxide thickness (about 22.8 angstroms + .3) for semiconductor wafers comprising a layer of Si above them. Data point 201 represents a value of gate oxide thickness (about 24 angstroms) for a semiconductor wafer comprising a layer of SiO2 above. As illustrated by the data points 201, 202,...215, it may be determined that gate oxide thickness increases as the materials change from Si to SiO2 and that based on a material placed above a semiconductor wafer during a wafer/semiconductor device manufacturing process a value of an electrical characteristic (e.g., gate oxide thickness) may be changed.

[0031] While embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.